CLAIMS

What is Claimed is:

1. An on-chip test apparatus comprising:

a first and a second data latch fabricated on-chip, each of said first and second data latches having a respective input and a respective output;

a test structure fabricated on-chip; and

a selective coupling means for selectively coupling the output of the first data latch to the input of the second data latch either directly or through the test structure.

2. The on-chip test apparatus as claimed in claim 1, the selective coupling means comprising:

a first multiplexer having a pair of first mux inputs and a first mux output, one of said pair of first mux inputs coupled to the first data latch output and to an input of the test structure, the other of said pair of first mux inputs coupled to an output of the test structure, and the first mux output coupled to the second data latch input.

3. The on-chip test apparatus as claimed in claim 2, the selective coupling means further comprising:

a second multiplexer having a pair of second mux inputs and a second mux output, one of said pair of second mux inputs coupled to the first data latch output, and the second mux output coupled to the second data latch input.

4. The on-chip test apparatus as claimed in claim 1, the selective coupling means comprising:

a first multiplexer having a pair of first mux inputs and a first mux output;

a second multiplexer having a pair of second mux inputs and a second mux output;

one of said pair of first mux inputs coupled to the first data latch output, the first mux output coupled to an input of the test structure and one of said pair of second mux inputs, the other of said pair of second mux inputs coupled to an output of the test structure, the second mux output coupled to the second data latch input.

5. The on-chip test apparatus as claimed in claim 3 wherein the other of said pair of first mux inputs is coupled to an inverted first data latch output.

6. The on-chip test apparatus as claimed in claim 3 wherein the other of said pair of first mux inputs is coupled to a predetermined test signal.

7. The on-chip test apparatus as claimed in claim 6 wherein the predetermined test signal comprises an inverted first data latch output.

8. An on-chip test apparatus comprising:

a first and a second data latch fabricated on-chip, each of said first and second data latches having a respective input and a respective output;

a test structure fabricated on-chip;

a first multiplexer having a pair of first mux inputs and a first mux output;

a second multiplexer having a pair of second mux inputs and a second mux output; and

one of said pair of first mux inputs coupled to the first data latch output, the other of said pair of first mux inputs coupled to an inverted first data latch output, the first mux output coupled to an input of the test structure and one of said pair of second mux inputs, the other of said pair of second mux inputs coupled to an output of the test structure, the second mux output coupled to the second data latch input.

9. A multi-stage on-chip test apparatus comprising:

a test stage comprising:

a data latch fabricated on-chip, said data latch having a data latch input and a data latch output;

a test structure fabricated on-chip, said test structure having a test input and a test output;

a first multiplexer having a pair of first mux inputs and a first mux output;

a second multiplexer having a pair of second mux inputs and a second mux output;

one of said pair of first mux inputs coupled to the data latch output and the other of said pair of first mux inputs coupled to an inverted data latch output, the first mux output

coupled to the test input and to one of said pair of second mux inputs, the other of said pair of second mux inputs coupled to the test output.

10. The on-chip test apparatus as claimed in claim 9 wherein a plurality of test stages are concatenated such that a subsequent test stage data latch input is coupled to a preceding test stage second mux output.

11. An on-chip test apparatus comprising:

an n-bit shift register fabricated on-chip, said shift register including n data latches;

n-1 test structures fabricated on-chip; and

selective coupling means associated with each pair of adjacent data latches for selectively coupling adjacent data latches either directly or via a respective test structure, wherein loading and unloading of test data occurs when the adjacent data latches are coupled directly and testing of the test structures occurs when the adjacent data latches are coupled through the test structures.

12. The on-chip test apparatus as claimed in claim 11, each of said selective coupling means comprising:

a first multiplexer having a pair of first mux inputs and a first mux output;

a second multiplexer having a pair of second mux inputs and a second mux output; and

one of said pair of first mux inputs coupled to a first data latch output, the other of said pair of first mux inputs coupled to an inverted first data latch output, the first mux output coupled to an input of a respective one of the test structures and one of said pair of second mux inputs, the other of said pair of second mux inputs coupled to an output of the respective one of the test structures, the second mux output coupled to a second data latch input.

13. A method for conducting an on-chip test on an IC chip comprising the sequential steps of:

providing an IC chip;

fabricating a first and a second data latch on said IC chip, each of said first and second data latches having a respective input and a respective output;

fabricating a test structure on said IC chip; and

providing a selective coupling means and selectively coupling the output of the first data latch to the input of the second data latch either directly or through a test structure.

14. The method for conducting on-chip test according to claim 13 further comprising the steps of:

providing a first multiplexer having a pair of first mux inputs and a first mux output, coupling one of said pair of first mux inputs to the first data latch output and to an input of the test structure, coupling the other of said pair of first mux inputs to an output of the test structure, and coupling the first mux output to the second data latch input.

15. The method for conducting an on-chip test according to claim 13 further comprising the step of:

providing a second multiplexer having a pair of second mux inputs and a second mux output, coupling one of said pair of second mux inputs to the first data latch output, and coupling the second mux output to the second data latch input.